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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,071	12/09/2003	Eugene James Nosowicz	ROC920030350US1	3763

7590 03/08/2006

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,071	NOSOWICZ, EUGENE JAMES	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Paul Dinh

Paul Dinh

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 12/09/2003. Claims 1-16 are pending.

Claim Objections

Claims 2 and 12 are objected to because of the following informalities: the recited " the steps of providing RVT transistors to implement output buffer transistors" lacks of antecedent basis. Appropriate correction is required.

Claims 3 and 13 are objected to because of the following informalities: the recited "the steps of identifying logic blocks used in loading data into the latch circuit " lacks of antecedent basis. Appropriate correction is required.

Claim 4 is objected to because of the following informalities: the recited "the steps of identifying logic blocks used in each data clock stage" lacks of antecedent basis. Appropriate correction is required.

Claims 5 and 15 are objected to because of the following informalities: the recited "the steps of identifying logic blocks used only during testing in the latch circuit " lacks of antecedent basis. Appropriate correction is required.

Claims 6 and 16 are objected to because of the following informalities: the recited "the steps of identifying logic blocks used to maintain the contents of latches in the latch circuit " lacks of antecedent basis. Appropriate correction is required.

Claim 14 is objected to because of the following informalities: the recited "the steps of identifying logic blocks used in a data clock stage" lacks of antecedent basis. Appropriate correction is required.

Specification

The abstract of the disclosure is objected to because the title is included in the abstract. The title should be removed from the abstract page. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by **Sani et al.** (US Patent No. 6794914).

Referring to claim 1 and similarly recited claim 11, Sani et al. disclose a method for implementing enhanced performance with reduced quiescent power dissipation using mixed threshold CMOS devices in latch circuit designs comprising the steps of:

identifying logic blocks in critical data and clock paths (signal path) of a latch circuit (Fig. 2; elements 210, 220, 240, 250; col. 6, ll. 53-62);

substituting a low voltage threshold (LVT) transistor to replace each regular voltage threshold (RVT) transistor for use in said identified logic blocks in the critical data and clock paths (Fig. 2; elements 210, 220, 240, 250; col. 6, ll. 53-62); and

selectively implementing non-critical sections of the latch circuit with RVT transistors, or low leakage (LLD) transistors (Fig. 2; elements 230 and 260 ; col. 6, ll. 53-62).

Referring to claim 2 and similarly recited claim12, Sani et al. disclose a method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 includes the steps of providing RVT transistors to implement output buffer transistors (Fig. 3, element 378; col. 10, ll. 61-67).

Referring to claim 3 and similarly recited claim 13, Sani et al. disclose a method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 wherein the step of identifying logic blocks in critical data and clock paths of the latch circuit includes the steps of identifying logic blocks used in loading data into the latch circuit (Fig.2, element 210; col. 6, ll. 53-62).

Referring to claim 4 and similarly recited claim 14, Sani et al. disclose a method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 3 includes the steps of identifying logic blocks used in each data clock stage (Sani et al., Figs. 2-3; col. 5, ll. 32-col. 6, ll. 67).

Referring to claim 5 and similarly recited claim 15, Sani et al. disclose a method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 wherein the step of selectively implementing non-critical sections of the latch circuit with RVT transistors, or low leakage (LLD) transistors includes the steps of identifying logic blocks used only during testing in the latch circuit (Fig. 3; col. 7, ll. 1- col. 10, ll. 67); and selectively implementing the identified logic

blocks used only during testing with RVT transistors, or low leakage (LLD) transistors (Fig. 3; col. 7, ll. 1- col. 10, ll. 67).

Referring to claim 6 and similarly recited claim 16, Sani et al. disclose a method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 wherein the step of selectively implementing non-critical sections of the latch circuit with RVT transistors, or low leakage (LLD) transistors includes the steps of identifying logic blocks used to maintain the contents of latches in the latch circuit (Fig. 3, logic blocks in elements 340 and 360; col. 7, ll. 1- col. 10, ll. 67); and selectively implementing the identified logic blocks used to maintain the contents of latches with RVT transistors, or low leakage (LLD) transistors (Fig. 3, logic blocks in elements 340 and 360; col. 7, ll. 1- col. 10, ll. 67).

Referring to claim 7, Sani et al. disclose a latch circuit for implementing enhanced performance with reduced quiescent power dissipation comprising:

critical data and clock paths (Fig. 2; paths that connected elements 210, 220, 240, and 250; col. 6, ll. 53-62);

non-critical sections (Fig. 2; sections include elements 230 and 260; col. 6, ll. 53-62);

a low voltage threshold (LVT) transistor being used only in said critical data and clock paths (Fig. 2; elements 210, 220, 240, 250; col. 6, ll. 53-62); and

said non-critical sections being implemented with regular voltage threshold (RVT) transistors, or low leakage (LLD) transistors (Fig. 2; elements 230 and 260; col. 6, ll. 53-62).

Referring to claim 8, **Sani et al.** disclose a latch circuit for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 7 includes said RVT transistors used for output buffer transistors (Fig. 3, element 378; col. 10, ll. 61-67).

Referring to claim 9, **Sani et al. disclose** a latch circuit for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 7 wherein said critical data and clock paths include multiple critical path logic blocks, each critical path logic block implemented with said LVT transistors (Fig. 2, elements 210, 220, 240, and 250; col. 6, ll. 53-62).

Referring to claim 10, **Sani et al.** disclose a latch circuit for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 7 wherein said non-critical sections include logic blocks used for testing (Fig. 3, elements 311 and 321) and to maintain the contents of latches in the latch circuit (Fig. 3, logic blocks in elements 340 and 360; col. 7, ll. 1- col. 10, ll. 67).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To

Patent Examiner

AU 2825

PAUL DINH

PRIMARY EXAMINER